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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| | | | |
|------------------------------|--------------------------------------|--|--|
| Office Action Summary | Application No. 09/392,034 | Applicant(s) GONZALEZ ET AL. | |
| | Examiner Anh D. Mai | Art Unit 2814 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 June 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-22,24-27,31-40,42 and 43 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-22,24-27,31-40,42 and 43 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 September 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 3, 2008 has been entered.

Status of the Claims

2. Amendment filed April 3, 2008 is acknowledged. Claims 1, 5-7, 9, 11, 14, 18, 24-27, 31, 35-40, 42 and 43 have been amended. Claims 1, 3-22, 24-27, 31-40, 42 and 43 are pending.

Specification

3. The amendment to the specification filed April 3, 2008 is acknowledged.

However, as filed, the specification does not contain paragraph numbers, i.e., [0051], but rather pages and lines. Therefore, the current amendment should be directed to page 15, and paragraph beginning on line 11, instead of [0051].

Appropriate action is required.

4. The amendment filed April 3, 2008 is objected to under 35 U.S.C. 132(a) because it *introduces new matter into the disclosure*. 35 U.S.C. 132(a) states that no amendment shall

Art Unit: 2814

introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

“For example, etching may be performed using an etch recipe that etches the reduced island 52 faster than the isolation structure 48 **by a ratio in a range of from about 1:1 to about 2:1 or more specially, by a ratio of about 1.3:1 to about 1.7:1**”.

Applicant is required to cancel the new matter in the reply to this Office Action.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “**implanting ions** in the plurality of isolation trench **in a direction substantially orthogonal to a plan of the oxide layer**” must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

Art Unit: 2814

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Note that, regions 34 as shown in Figs. 5-9, signify a vertical implantation or implantation in direction perpendicular to the oxide layer 14, not orthogonal.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 20 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation “**implanting ions in the plurality isolation trenches** (claim 18) **and further comprising forming a doped region** below the termination of each isolation trench within the semiconductor substrate (claim 20)” (emphasis added) in the application as filed.

Note that the specification only supports for **one** implantation, not two.

Applicant is required to cancel the new matter in the reply to this Office Action.

Art Unit: 2814

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1, 3-9, 11, 12, 14-22, 24-26, 31-40, 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor (U.S. Patent No. 6,097,072) in view of Park et al., (U.S. Patent No. 5,858,858) both of record, and G. Fuse et al., A New Isolation Method with Boron-Implanted Sidewalls for Controlling Narrow-Width Effect, IEEE 1987, pp. 356-360.

With respect to claim 1, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a first dielectric layer (344) upon an oxide layer (340) over a semiconductor substrate (120);

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer (340);

forming a second dielectric layer (352) over the first dielectric layer (344) and in contact with the plurality of exposed areas of the oxide layer (340);

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) at peripheral edges of the plurality of exposed areas of the oxide layer in contact with lateral edges of the first dielectric layer (344);

Art Unit: 2814

removing a portion of material from the plurality of areas of the oxide layer at locations between adjacent portions of the plurality of spacers (356) to form a plurality of isolation trenches (360) extending into the semiconductor substrate (120); depositing a conformal layer (364) in each isolation trench, the conformal layer extending over remaining portions of the oxide layer in contact with a corresponding pair of the spacers (356), wherein the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364); removing portions of the conformal layer (364) overlying the remaining portions of the oxide layer (340) by planarizing the conformal layer (364) at least to the first dielectric layer (344) and each spacer (356) such that an upper surface for each isolation trench (376) is co-planar to the other upper surfaces; and wherein the conformal layer (364) comprises a material that is electrically insulative extends continuously between and within the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *forming a liner upon the sidewall of each isolation trench; heat treating the conformal layer and implanting ions in the isolation trenches.*

Art Unit: 2814

However, Park teaches a method of forming a microelectronic structure including forming a liner (22) upon the sidewall of each isolation trench (20) to remove damage caused by the trench-etch. (See Fig. 5).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Park to remove the damage caused by the trench-etch.

Park further teaches the microelectronic is then heat treated to densify the conformal layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to densify the conformal layer of Omid-Zohoor '072 as taught by Park to decrease the etch rate of the conformal layer so that dishing is avoided.

Regarding the heat treating, in view of Park, the heat treating would have obviously fused the oxide layer (340), liner (22), spacer (356) and conformal layer (364).

Further, G. Fuse et al., teaches a new isolation method including implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including implanting ions in the isolation trench in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

Art Unit: 2814

With respect to claim 3, forming the liner (22) upon the sidewall of each isolation trench of Park includes thermally grown oxide on the semiconductor substrate.

With respect to claim 4, in view of G. Fuse et al., the forming the liner upon the sidewall of the isolation trench comprises depositing a composition of matter. (See Fig. 1b).

With respect to claim 5, in view of G. Fuse et al., implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer comprises forming a doped region below the termination of each of the plurality of the isolation trenches within the semiconductor substrate.

With respect to claim 6, the removing portions of the conformal layer (364) overlying the remaining portions of the oxide layer of Omid-Zohoor comprises removing portions of the conformal layer (364) overlying the remaining portions of the oxide layer (340) by CMP. (See Fig. 3M, col. 4, ll. 47-62).

With respect to claim 7, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming a first dielectric layer (344) upon an oxide layer (340) over a semiconductor substrate (120);

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer (340);

forming a second dielectric layer (352) over the first dielectric layer (344) in contact with the plurality of exposed areas of the oxide layer (340);

Art Unit: 2814

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) at peripheral edges of the plurality of exposed areas of the oxide layer (340) in contact with lateral edges of the first dielectric layer (344);

removing a portion material from the plurality of areas of the oxide layer at locations between adjacent portion of the plurality of spacers to form a plurality of isolation trenches (360) extending into the semiconductor substrate (120);

depositing a conformal layer (364) filling each the isolation trench (360), the conformal layer extending over the remaining portions of the oxide layer (340) in contact with the corresponding pair of the spacers (356), wherein the depositing is carried out to the extent of filling each of the isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364);

removing portions of the conformal layer that overlie the remaining portions of the oxide layer by planarizing the conformal layer (364) to form an upper surface for each of the isolation trench (360) that is co-planar to the other upper surfaces;

wherein:

the conformal layer (364) comprises a material that is electrically insulative and extends continuously between and within the plurality of isolation trenches (360);

the conformal layer (364) and the spacers (356) form the upper surface for each isolation trench, each upper surface being formed from the conformal layer (364) and the spacer (356) and being situated above the oxide layer (340); and

Art Unit: 2814

the first dielectric layer (344) is in contact with at least a pair of the spacers (356) and the oxide layer (340). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *rounding the top edge of each of the isolation trenches; heat treating the conformal layer and implanting ions in the isolation trenches.*

However, Park teaches a method of forming a microelectronic structure including forming a liner (22) upon the sidewall of each isolation trench (20) to remove damage caused by the trench-etch. (See Fig. 5).

Note that, the forming of the liner (22) by thermal oxidation of the substrate inherently rounding the top edges of the isolation trenches. This is well known in the art. See Wolf et al. of record.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Park to remove the damage caused by the trench-etch, thus rounding the top edge at the same time.

Park further teaches the microelectronic is then heat treated to densify the conformal layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to densify the conformal layer of Omid-Zohoor '072 as taught by Park to decrease the etch rate of the conformal layer so that dishing is avoided.

Art Unit: 2814

Regarding the heat treating, in view of Park, the heat treating would have obviously fused the oxide layer (340), liner (22), spacer (356) and conformal layer (364).

Further, G. Fuse et al., teaches a new isolation method including implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including implanting ions in the isolation trench in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

With respect to claim 8, the method of Omid-Zohoor '072 further includes: removing the oxide layer (340) upon a portion of the surface of semiconductor substrate (120); (Fig. 3O); and forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate. (See Fig. 3P).

With respect to claim 9, removing portions of the conformal layer (340) of Omid-Zohoor '072 comprises etching the material using an etch that etches the conformal layer (340) faster than the first dielectric layer (344). This is evident by the etch of Omid-Zohoor '072 or Park '858 formed a planar surface, which meets the range of 1:1.

Note that the specification contains no disclosure of either the *critical nature of the claimed etch rate of the conformal layer (oxide) as compared to that of the first dielectric layer (nitride)* of any unexpected results arising therefrom. Where patentability is aid to base upon

Art Unit: 2814

particular chosen etch rate or upon another variable recited in a claim, the Applicant must show that the chosen etch rate are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

More over, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges **involves only routine skill in the art**. *In re Aller*, 105 USPQ 223.

With respect to claim 11, removing portions of the conformal layer (364) overlying the remaining portions of oxide layer (340) of Omid-Zohoor '072 includes a chemical mechanical planarization, CMP, wherein the conformal layer (364), the spacers (356), and the first dielectric layer (344) form a planar first upper surface; (Fig. 3M); and etching to form a second upper surface situated above the oxide layer (340). (Fig. 3N).

With respect to claim 12, the etching to form a second upper surface of Omid-Zohoor '072 includes etching using an etch recipe that etches the first dielectric layer (nitride 344) faster than the oxide layer (340, 356). (See Fig. 3N). This is evident by the etch of Omid-Zohoor '072 or Park '858 formed a planar surface, which meets the range of 1:1.

Note that the specification contains no disclosure of either the *critical nature of the claimed etch rate of the conformal layer (oxide) as compared to that of the first dielectric layer (nitride)* of any unexpected results arising therefrom. Where patentability is aid to base upon particular chosen etch rate or upon another variable recited in a claim, the Applicant must show

Art Unit: 2814

that the chosen etch rate are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

More over, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges **involves only routine skill in the art**. *In re Aller*, 105 USPQ 223.

With respect to claim **14**, as best understood by Examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a silicon nitride layer (344) upon the oxide layer (340);

selectively removing the silicon nitride layer (344) to expose a plurality areas of the oxide layer (340);

forming a first silicon dioxide layer (352) over the silicon nitride layer (344), and in contact with the plurality of exposed areas of the oxide layer (340);

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) at the peripheral edges of the plurality of exposed areas of the oxide layer in contact with the lateral edges of the silicon nitride layer (344);

removing a portion material from the plurality of areas at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches (360) into the semiconductor substrate (120);

forming a corresponding electrically active region below the termination of each isolation trench (360) within the semiconductor substrate;

Art Unit: 2814

depositing a conformal second silicon dioxide layer (364) filling each isolation trench (360), the conformal second silicon dioxide layer within each isolation trench and extending over remaining portions of the oxide layer (340) in contact with a corresponding pair of the spacers (356), and the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and the silicon nitride layer (344) so as to define an upper surface contour of the conformal second silicon dioxide layer (364); and removing portions of the conformal second silicon dioxide layer (364) by planarizing the conformal second silicon dioxide layer (364) and the spacers (356) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces, wherein an electrically insulative material extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *forming a liner upon the sidewall of each isolation trench; heat treating the conformal layer and implanting ions in the isolation trenches.*

The same reasoning as discussed in claim 1 above also applies here.

With respect to claim 15, in view of Park, forming the liner (22) upon the sidewall of each isolation trench includes thermally grown oxide upon the sidewall of the semiconductor substrate.

Art Unit: 2814

With respect to claim 16, in view of G. Fuse et al., forming a liner upon the sidewall of each isolation trench comprises forming a liner composed of silicon nitride. (See Fig. 1b).

With respect to claim 17, the process of Omid-Zohoor '072 further includes: removing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120); (Fig. 3O); and forming a gate oxide layer (380) upon the portion of the surface of semiconductor substrate (120). (See Fig. 3P).

With respect to claim **18**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer;

forming a second dielectric layer (352) conformally over the polysilicon layer the first dielectric layer (344) and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356)

at the peripheral edges of the plurality of exposed areas of the oxide layer, in contact with lateral edges of the first dielectric layer (344);

removing a portion of material from the plurality of areas of the oxide layer at locations between adjacent portions of the plurality of spacers (356) to form a plurality of

Art Unit: 2814

isolation trenches (360) extending into and terminating within the semiconductor substrate (120);

depositing a conformal third layer (364) filling each isolation trench (360), the conformal third layer extending over remaining portion of the oxide layer in contact with a corresponding pair of the spacers (356), wherein depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

removing portions of the conformal third layer (364) by planarizing the conformal third layer (364) to form an upper surface for each isolation trench that is co-planar to the other upper surface; and

wherein a material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *removing the polysilicon layer to expose plurality of areas of the oxide layer; rounding the top edge of each of the isolation trenches; heat treating the conformal layer; and implanting ions in the isolation trenches.*

Art Unit: 2814

Regarding the removing of polysilicon layer to expose the oxide layer, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer.

However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines 14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

Regarding the limitations rounding the top edge of each of the isolation trenches; heat treating the conformal layer; and implanting ions in the isolation trenches, the same reasoning as discussed in claim 7 above also applies here.

With respect to claim 19, removing portions of the conformal third layer (364) of Omid-Zohoor '072 includes removing portions of the conformal layer (364) by CMP.

With respect to claim 20, as best understood by Examiner, in view of G. Fuse et al., the implanting ions in the plurality of isolation trenches forming a doped region below the termination of each isolation trenches within the semiconductor substrate.

Art Unit: 2814

With respect to claim 21, in view of Park, the rounding the top edges of each of the isolation trenches comprises forming a liner (22) upon the sidewall of the isolation trench (20), the liner (22) being confined preferentially within each isolation trench and extending from an interface thereof with the oxide layer (12A) to the termination of the isolation trench (20) within the semiconductor substrate, and wherein the conformal third layer is composed of electrically insulative material.

With respect to claim 22, the forming liner (22) upon the sidewall of each isolation trench of Park includes forming a thermally grown oxide upon the sidewall of the semiconductor substrate.

With respect to claim **24**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer;

forming a second dielectric layer (352) over the polysilicon layer, the first dielectric layer (344) and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) at the peripheral edges of the plurality of exposed areas of the oxide layer, in contact with the lateral edges of the first dielectric layer (344);

Art Unit: 2814

removing a plurality of material from the plurality of exposed areas of the oxide layer at locations between adjacent portions of the plurality of spacers to form a plurality of isolation trenches (360) extending into and terminating within the semiconductor substrate (120);

depositing a conformal third layer (364) filling each isolation trench (360), the conformal third layer extending over the remaining portions of the oxide layer in contact with a corresponding pair of the spacers (356), wherein the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

removing portions of the conformal layer (364) by planarizing the conformal third layer (364) to form an upper surface for each isolation trench that is co-planar to the other upper surface;

wherein the conformal third layer (364) is an electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein the upper surface of each isolation trench is formed from the conformal third layer (364), the spacers (356), and the first dielectric layer (344); and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364), and the plurality of isolation trench. (See Figs. 3A-M).

Art Unit: 2814

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly *disclosing removing the polysilicon layer to expose plurality of areas of the oxide layer; implanting ions in the plurality of isolation trenches; and heat treating the conformal layer.*

The same reasoning as discussed in claim 18 also applies here.

With respect to claim **25**, as best understood by Examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer;

forming a second dielectric layer (352) over the first dielectric layer (344) and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) at peripheral edges of the plurality of exposed areas of the oxide layer in contact with

the lateral edges of the first dielectric layer (344);

removing a portion of material from the plurality of exposed areas of the oxide layer at locations between adjacent portions of the plurality of spacers (356) to form a

plurality of isolation trenches (360) extending into and terminating within the semiconductor substrate (120);

Art Unit: 2814

depositing a conformal third layer (364) filling each isolation trench (360), the conformal third layer extending over the remaining portions of the oxide layer in contact with a corresponding pair of the spacers (356), wherein the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal third layer (364);

removing portions of the conformal third layer (364) overlying the remaining portions of the oxide layer by planarizing the conformal third layer (364) to form an upper surface for each isolation trench that is co-planar to the other upper surface;

exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120);

forming between the plurality of isolation trenches, and confined in the space therebetween, a layer composed of polysilicon upon the oxide layer in contact with the pair of the spacers (356);

selectively removing the conformal third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces; and

wherein a material that is electrically insulative (364) extends continuously between and within the plurality of isolation trenches. (See Fig. 3A-M).

Art Unit: 2814

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *removing the polysilicon layer to expose plurality of areas of the oxide layer; rounding the top edge of each of the isolation trenches; heat treating the conformal layer; and implanting ions in the isolation trenches.*

The same reasoning as discussed in claim 18 also applies here.

With respect to claim **26**, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer upon a semiconductor substrate (120);

forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer (344) to expose a plurality of areas of the oxide layer;

forming a second dielectric layer (352) over the polysilicon layer and the first dielectric layer (344) and in contact with the plurality of exposed areas of the oxide layer;

selectively removing the second dielectric layer (352) to form a plurality of spacers (356) at the edges of the plurality of exposed areas of the oxide layer in contact with lateral

edges of the first dielectric layer (344);

removing material from the plurality of exposed areas of the oxide layer at locations

between adjacent portions of the plurality of spacers (356) to form a plurality of isolation trenches (360) extending into and terminating within the semiconductor substrate (120);

Art Unit: 2814

depositing a conformal third layer (364) filling each isolation trench (360), the conformal third layer extending over the remaining portions of the oxide layer in contact with a corresponding pair of the spacers (356), wherein the depositing is carried out to the extend of filling each isolation trench (360) and extending over the spacers (356) and over the first dielectric layer (344) so as to define an upper surface contour of the conformal layer (364);

removing portions of the conformal third layer (364) overlying the remaining portions of the oxide layer by planarizing the conformal third layer (364) to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surface using an etch recipe that etches the conformal third layer (364) and the spacers (356) faster than the first dielectric layer (344) by a ratio of from about 1:1 to about 2:1; wherein a material that is electrically insulative (364) extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the conformal third layer (364) and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *removing the polysilicon layer to expose plurality of areas of the oxide layer; rounding the top edge of each of the isolation trenches; heat treating the conformal layer; and implanting ions in the isolation trenches.*

The same reasoning as discussed in claim 18 also applies here.

Regarding the etch ratio in the range from about 1:1 to about 2:1, since the etch of Omid-Zohoor results in a planar surface, Fig. 3M, the etch ratio is at least 1:1. This is evident by the etch of Omid-Zohoor '072 or Park '858 formed a planar surface, which meets the range of 1:1.

Note that the specification contains no disclosure of either the *critical nature of the claimed etch ratio of from about 1:1 and 2:1* of any unexpected results arising therefrom. Where patentability is aid to base upon particular chosen etch ratio or upon another variable recited in a claim, the Applicant must show that the chosen etch rate are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

More over, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges **involves only routine skill in the art**. *In re Aller*, 105 USPQ 223.

With respect to claim **31**, as best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

- forming a pad oxide layer upon a semiconductor substrate (120);
- forming polysilicon layer upon the oxide layer; (see col. 4, ll. 14-16);
- forming a silicon nitride layer (344) upon the polysilicon layer;
- selectively removing the silicon nitride layer (344) to expose a plurality of areas of the pad oxide layer;

Art Unit: 2814

forming a first silicon dioxide layer (352) over the silicon nitride layer (344) and in contact with the exposed oxide layer at the plurality of exposed areas of the oxide layer;

selectively removing the first silicon dioxide layer (352) to form a plurality of spacers (356) at peripheral edges of the plurality of exposed areas of the oxide layer in contact with the lateral edges of the silicon nitride layer (344) and the polysilicon layer;

removing a portion of material from the plurality of exposed areas at locations between adjacent portions of the plurality of spacers (356) to form a plurality of isolation trenches (360) extending into and terminating within the semiconductor substrate (120), wherein each isolation trench of the plurality of isolation trenches is adjacent to and below a pair of the spacers (356) and is situated at a corresponding area of the plurality of areas;

depositing a conformal second layer (364) filling each isolation trench (360), the conformal second layer extending over the remaining portions of the pad oxide layer in contact with a corresponding pair of the spacers (356), wherein the depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the silicon nitride layer (344) so as to define an upper surface contour of the conformal second layer (364);

removing a portions of the conformal second layer (364) by planarizing the conformal second layer (364) and each of the spacers (356) to form an upper surface for each

Art Unit: 2814

isolation trench that is co-planar to the other upper surface and is situated above the pad oxide layer (340); and
wherein a material that is electrically insulative (364) extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *removing the first dielectric layer and the polysilicon layer to expose plurality of areas of the oxide layer; forming a corresponding doped region by implanting ions in the plurality of isolation trenches; forming a liner upon the sidewall of each isolation trench; and heat treating the conformal layer.*

The same reasoning as discussed in claim 18 also applies here.

With respect to claim 32, in view of Park or G. Fuse, each liner is a thermally grown oxide of the semiconductor substrate and the conformal second layer (364) is composed of an electrically insulative material.

With respect to claim 33, in view of G. Fuse, the liner is also composed of silicon nitride and wherein the conformal second layer of Omid-Zohoor is composed of an electrically insulative material.

With respect to claim 34, the method of Omid-Zohoor further comprises:
exposing the oxide layer (340) upon a portion of the surface of the semiconductor substrate (120);

Art Unit: 2814

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate (120); forming between the plurality of isolation trenches (360), and confined in the space therebetween, a layer composed of polysilicon (384) upon the gate oxide layer (380) in contact with the pair of the spacers (356); and selectively removing the layer composed of polysilicon (384) to form a portion of at least one of the upper surfaces. (See Fig. 3Q).

With respect to claim **35**, Omid-Zohoor teaches a method of forming a microelectronic structure substantially similar as claimed including:

forming a polysilicon layer upon an oxide layer overlying a semiconductor substrate (120); (col. 4, ll.14-16);

forming a first layer (344) upon the polysilicon layer;

selectively removing the first layer (344) to expose a plurality of areas of the oxide layer;

forming a plurality of isolation trenches (360) through the exposed oxide layer at the plurality of areas;

wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trenches, each isolation trench (360):

having a spacer (356) composed of a dielectric material upon the oxide layer

(340) in contact with the first layer (344) and the polysilicon layer;

extending from an opening thereto at the top surface of the semiconductor

substrate and below the oxide layer into and terminating within the

semiconductor substrate adjacent to and below the spacer;

Art Unit: 2814

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer in contact with the spacer (356), wherein the filling is performed by depositing the second layer, and depositing is carried out to the extent of filling each isolation trench (360) and extending over the spacers (356) and over the first layer (344) so as to define an upper surface contour of the second layer; and

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer, wherein the planar upper surface is formed by substantially simultaneously subjecting the entire upper surface contour of the second layer to planarizing process; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches (360). (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly *disclosing removing the first layer and the polysilicon layer to expose plurality of areas of the oxide layer; implanting ions in the plurality of isolation trenches; and heat treating the conformal layer.*

Regarding the removing of the first layer and the polysilicon layer to expose the oxide layer, although Omid-Zohoor '072 does not explicitly disclose removing the polysilicon layer to expose the oxide layer. However, Omid-Zohoor clearly teaches that a thin thermally-grown silicon oxide and a buffer polysilicon layer may be used for the pad oxide 340. (See col. 4, lines

Art Unit: 2814

14-16). Also, Omid-Zohoor clearly intended for the spacers (356) to be formed on the thermally-grown oxide layer (34). (See Figs. 3E-H).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to remove the first dielectric layer (344) and the polysilicon layer to expose the oxide layer as shown in Fig. 3E, without departing from the scope of Omid-Zohoor's invention, to form a T-shape isolation.

Further, G. Fuse et al., teaches a new isolation method including implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including implanting ions in the isolation trench in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

Furthermore, Park teaches a method of forming a microelectronic structure including heating treating to densify the conformal third layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to heat treat the conformal third layer of Omid-Zohoor '072 to densify it as taught by Park to decrease the etch rate of the conformal third layer so that dishing is avoided. Moreover, the heat treating of the substrate is obviously fused the oxide layer (340), the liner (22), spacer (356) and conformal layer (364).

With respect to claim **38**, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

forming a first layer (344) upon an oxide layer (340) overlying a semiconductor substrate (120);

selectively removing the first layer (344) to expose a plurality of areas of the oxide layer (340);

forming a plurality of isolation trenches (360) through the oxide layer (340) at the plurality of areas, wherein an electrically insulative material (364) extends continuously between and within the plurality of isolation trench, each isolation trench (360):

having a spacer (356) composed of dielectric material upon the oxide layer (340) in contact with the first layer (344);

extending from an opening thereto at top surface of the semiconductor substrate (120) and below the oxide layer (340) into and terminating within the semiconductor substrate adjacent to and below the spacer (356);

having a second layer (364) filling the isolation trench (360) and extending above the oxide layer (340) in contact with the spacer (356), wherein the filling is performed by depositing the second layer (364), and the depositing is carried out to the extend of filling each isolation trench and extending over the spacer (356) and over the first layer (344); so as to define an upper surface contour of the second layer (364); and

Art Unit: 2814

having a planar upper surface formed from the second layer (364) and the spacer (356) and being situated above the oxide layer (340), wherein the planar upper surface is formed by removing portions of second layer by planarizing the entire upper surface contour of the second layer (364); and wherein the microelectronic structure is defined at least in part by the plurality of spacers (356), the second layer (364), and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of explicitly *implanting ions in the plurality of isolation trenches; and heat treating the conformal layer*.

However, G. Fuse et al., teaches a new isolation method including implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including implanting ions in the isolation trench in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

Further, Park teaches a method of forming a microelectronic structure including heating treating to densify the conformal third layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to heat treat the conformal third layer of Omid-Zohoor '072 to densify it

Art Unit: 2814

as taught by Park to decrease the etch rate of the conformal third layer so that dishing is avoided. Moreover, the heat treating of the substrate is obviously fused the oxide layer (340), the liner (22), spacer (356) and conformal layer (364).

With respect to claims 36 and 39, in view of G. Fuse et al., the method further includes: doping the semiconductor substrate with a dopant having a first conductivity type; and wherein implanting ions in the plurality of isolation trenches in the direction substantially orthogonal to the plane of the oxide layer further includes: doping the semiconductor substrate below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one isolation trench of the plurality of isolation trenches. (See Fig. 2).

With respect to claims 37 and 40, in view of G. Fuse et al., the doped trench bottom has a width, each isolation trench has a width, and the width of each doped trench bottom is greater than the width of the respective isolation trench.

With respect to claim 42, Omid-Zohoor '072 teaches a method for forming a microelectronic structure substantially as claimed including:

forming a polysilicon layer upon an oxide layer overlying a semiconductor substrate
(120); (col. 4, ll. 14-16);

forming a first layer (344) upon the polysilicon layer;

forming a first isolation structure including:

Art Unit: 2814

- a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;
- a first isolation trench (360) extending into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and
- a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

- a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344) and the polysilicon layer;
- a first isolation trench (360) extending from into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and
- a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate (12) between the first and second isolation structures (360);

Art Unit: 2814

depositing a conformal second layer (364), the conformal layer filling the first and second isolation trenches and extending continuously over the remaining portions of the oxide layer in contact with the first and second spacers (356) of the respective first and second isolation structures (360), the depositing is carried out to the extent of filling each isolation trenches and extending over the spaces (356) and the first layer (344) so as to define an upper surface contour of the conformal second layer (364); planarizing portions of the upper surface contour of the conformal second layer; forming a planar upper surface from the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures and being situated above the oxide layer; wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer (364), and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *rounding the top edges of the isolation trenches; heat treating the conformal layer and doping the first and second isolation trenches by implanting ions.*

However, Park teaches a method of forming a microelectronic structure including forming a liner (22) upon the sidewall of each isolation trench (20) to remove damage caused by the trench-etch. (See Fig. 5). Note that, forming the liner (22) of Park by thermal oxidation of the semiconductor substrate inherently rounding the top edges of the isolation trench (20).

Art Unit: 2814

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Park to remove the damage caused by the trench-etch.

Park further teaches the microelectronic is then heat treated to densify the conformal layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to densify the conformal layer of Omid-Zohoor '072 as taught by Park to decrease the etch rate of the conformal layer so that dishing is avoided.

Regarding the heat treating, in view of Park, the heat treating would have obviously fused the oxide layer (340), liner (22), spacer (356) and conformal layer (364).

Further, G. Fuse et al., teaches a new isolation method including implanting ions in the plurality of isolation trenches in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including implanting ions in the isolation trench in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

With respect to claim **43**, Omid-Zohoor teaches a method for forming a microelectronic structure substantially as claimed including:

Art Unit: 2814

forming a first layer (344) upon an the oxide layer (340) overlying a semiconductor substrate (120);

forming a first isolation structure (360) including:

- a first spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer (344);

- a first isolation trench (360) extending into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

- a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure (360) including:

- a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer (344);

- a first isolation trench (360) extending into and terminating within the semiconductor substrate adjacent to and below the first spacer (356), wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge; and

- a second spacer (356) composed of a dielectric material upon the oxide layer (340) in contact with the first layer, the second spacer of the second isolation

Art Unit: 2814

structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

depositing a conformal second layer (364), comprising an electrically insulative material, to fill the first and second isolation trenches (360) and extending continuously over the remaining portions of the oxide layer (340) in contact with the first and second spacers (356) of the respective first and second isolation structures, wherein the depositing is carried out to the extent of filling each isolation trench and extending over the spaces (356) and the first layer (344) so as to define an upper surface contour of the conformal second layer (364);

planarizing the conformal second layer (364) and the first and second spacers (356) of the respective first and second isolation structures to form a planar upper surface. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all the features of the claim with the exception of *forming the isolation trenches having rounded top edges; heat treating the conformal layer; and doping the first and second isolation trenches by implanting ions.*

However, Park teaches a method of forming a microelectronic structure including forming a liner (22) upon the sidewall of each isolation trench (20) to remove damage caused by the trench-etch. (See Fig. 5). Note that, forming the liner (22) of Park by thermal oxidation of the semiconductor substrate inherently rounding the top edges of the isolation trench (20).

Art Unit: 2814

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the liner upon the sidewall of each isolation trench of Omid-Zohoor '072 as taught by Park to remove the damage caused by the trench-etch.

Park further teaches heat treating to densify the conformal layer (24). (See col. 3, lines 46-48).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to densify the conformal layer of Omid-Zohoor '072 by heat treating as taught by Park to decrease the etch rate of the conformal layer so that dishing is avoided.

Regarding the heat treating, in view of Park, the heat treating would have obviously fused the oxide layer (340), liner (22), spacer (356) and conformal layer (364).

Furthermore, G. Fuse et al., teaches a new isolation method including doping the isolation trenches by implanting ions in a direction substantially orthogonal to a plane of the oxide layer forming a channel stop. (See Fig. 2).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to form the microelectronic structure of Omid-Zohoor '072 including doping the first and second isolation trench by implanting ions in a direction substantially orthogonal to a plane of the oxide layer as taught by G. Fuse to control the narrow-width effect.

8. Claims 9, 10, 12, 13 and 27 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072, Park and G. Fuse et al., as applied to claims 7, 11 and 26 above, and further in view of Miyashita et al. (U.S. Patent No. 6,069,083) of record.

Art Unit: 2814

Omid-Zohoor teaches planarizing the conformal third layer (364) by an etch using an etch recipe that etches the conformal third layer (364) and the spacers (356) faster than the first dielectric layer (344).

Thus, Omid-Zohoor is shown to teach all the features of the claim with the exception of explicitly utilizing a ratio in the range from about 1:1 to about 2:1 or about 1.3:1 to about 1.7:1.

However, Miyashita teaches planarizing the conformal layer (6) by an etch using an etch recipe that etches the conformal layer (6) faster than the first dielectric layer (2) by a ratio in a range from about 1 (1:1) to about 3 (3:1), which encompasses the claimed ranges (1:1 to 2:1 and 1.3:1 to 1.7:1).

Note that the specification contains no disclosure of either the *critical nature of the claimed etch ratio of from about 1:1 and 2:1 or from about 1.3:1 to 1.7:1* of any unexpected results arising therefrom. Where patentability is aid to base upon particular chosen etch ratio or upon another variable recited in a claim, the Applicant must show that the chosen etch rate are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention was made to remove portions of the conformal layer of Omid-Zohoor using an etch recipe as taught by Miyashita to form a planar surface.

More over, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges **involves only routine skill in the art**. *In re Aller*, 105 USPQ 223.

Response to Arguments

9. Applicant's arguments with respect to amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 8:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Anh D. Mai/
Primary Examiner, Art Unit 2814